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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/536,927	03/27/2000	Andrew M. Hawryluk	3521.125(ALJ)	3973

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EXAMINER

THOMAS, TONIAE M

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 03/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/536,927

Applicant(s)

HAWRYLUK ET AL.

Examiner

Toniae M. Thomas

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 February 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-74 is/are pending in the application.
- 4a) Of the above claim(s) 26 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 27-52 is/are allowed.
- 6) ☒ Claim(s) 1, 2, 14, 20-25, 53, 61 and 69-74 is/are rejected.
- 7) ☒ Claim(s) 3-13, 15-19, 54-60 and 62-68 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 March 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 21 February 2003 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. *Claims 1, 2, 14, 21-23, 25, 53, 61, 70-72, and 74 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsukamoto (US 5,399,506 B1).*

Tsukamoto discloses a method comprising the following step substantially as claimed: annealing at least one region 21A/21B of a semiconductor substrate 11 while minimizing the diffusion of dopant atoms during activation by using a pulsed beam of particles having a duration between 10^{-10} to 10^{-4} seconds (col. 4, lines 28-34 and lines 42-55).

The substrate includes an amorphous region 21A, 21B positioned in contact with the substrate 11, and the particle beam heats the amorphous region to convert the

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amorphous region into a crystalline region. The ion implantation step used to form the source and drain regions 21A, 21B forms amorphous regions in the substrate. The particle beam heats the amorphous region to convert the amorphous region into a crystalline region (col. 4, lines 42-44).

The particles are produced from a gas including xenon (col. 4, lines 33-35).

The substrate includes a semiconductor material, silicon (col. 3, lines 57-60).

The substrate includes dopant atoms, and the particle beam heats and melts the substrate so that the dopant atoms are incorporated into the substrate on recrystallization (col. 4, lines 42-47).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. *Claims 20 and 69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukamoto.*

As discussed above, Tsukamoto discloses the step of annealing at least one region of a semiconductor substrate using a pulsed beam of particles. The energy of the pulse is 0.7 Joules/cm² (col. 4, lines 33-35). Tsukamoto does not teach that the energy dose of the pulse is from 0.1 to 1.0 joules/cm². However, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use an

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energy in the range of from 0.1 to 1.0 joules/cm², since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art (see *In re Aller, Lacey, and Hall* 105 USPQ 233 (CCPA 1955)).

4. *Claims 24 and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukamoto in view of Wolf (Silicon Processing for the VLSI Era - Vol. 2).*

Tsukamoto does not teach that the substrate includes a relatively thin layer of semiconductor material on an insulative material (SOI).

Wolf teaches using an SOI substrate in place of bulk substrate (pp. 66-78).

SOI substrates offer several advantages over bulk silicon substrates. As an example, SOI substrate eliminates parasitic field FET between adjacent devices. Thus, LOCOS isolation processes are not needed (page 67, 3rd par.).

It would have been obvious to one having ordinary skill in the art, at the time the invention was made, to form the substrate of Tsukamoto, such that it comprises a relatively thin layer of semiconductor material on an insulative material, as taught by Wolf, because an SOI substrate eliminates the need for LOCOS isolation areas 12 (Tsukamoto – fig. 1A).

Allowable Subject Matter

5. Claims 27-52 are allowable. Claims 3-13, 15-19, 54-60, and 62-68 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in

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independent form including all of the limitations of the base claim and any intervening claims.

Claims 27-51 are allowable because the prior art of record does not anticipate or render obvious a method substantially as claimed, wherein the pulsed beam comprises charged particles. The pulse is a laser light. Claim 52 is allowable because the prior art of record does not anticipate or render obvious a method substantially as claimed, wherein dopant atoms are implanted into the substrate at such that the dose and pulse duration imparted by the dopant atoms is sufficient to raise the temperature of the substrate atoms to permit annealing of the dopant atoms.

Claims 3-13, 15-19, 54-60, and 62-68 would be allowable over the prior art of record if rewritten as discussed above because the prior art of record does not anticipate or render obvious a method substantially as claimed, wherein the pulsed beam includes charged particles, neutral atoms, alpha particles, or a dopant atomic species.

References Cited

John et al. (US 4,402,762 B1) is cited in this action as art of interest because the reference teaches a method wherein an amorphous or germanium film is modified using a bombardment of ions or atoms (col. 3, lines 53-63). Nishihara et al. (2002/0031889 A1) is cited as art of interest because the reference discloses a method for forming a semiconductor device, wherein the method includes irradiating the substrate with electron beams or charged particles (par. [0036]).

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Response to Arguments

6. Applicant's arguments with respect to claims 1 and 53 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (703) 305-7646. The examiner can normally be reached on Monday through Thursday, and alternating Fridays, from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JMJ

March 23, 2003


AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800